REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated May 17, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-15 are under consideration in this application. Claims 1 and 5 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention.

Additional Amendments

The claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over US Pat. No. 5,091,784 to Someya et al. (hereinafter "Someya")in view of US Pat. No. 6,144,355 to Murata et al. (hereinafter "Murata"), further in view of US Pat. No. 6,211,849 to Sasaki et al. (hereinafter "Sasaki"), and further in view of US Pat. No. 5,754,838 to Shibata at al. (hereinafter "Shibata"). This rejection has been carefully considered, but is most respectfully traversed.

The liquid crystal display device of the invention (Embodiment 1 in Fig. 2 and Embodiment 2 in Fig. 23; Fig. 12), as now recited in claim 1, includes a liquid crystal display panel 100, a plurality of cascade-connected liquid crystal drive circuits 130, 140 (Fig. 1) for sequentially transferring a signal (Fig. 1; page 1, third line to the bottom; "*the display data and clock signal as sent out of the timing controller will be delivered and passed between respective drain drivers in a one-by-one manner*" page 3, lines 17-19), and a plurality of signal lines (Fig. 1, not numbered) formed over an edge portion of the liquid crystal display panel for

transmitting a signal between any two of the drive circuits. Each of the drive circuits comprises: an image input terminal connected with one of the signal lines to receive an external image signal ("Display Data Signal Input": D1-D7, 2nd row of Fig. 12) being input thereto as an internal image signal into said each of the liquid crystal drive circuits; a clock compensation circuit 200 (e.g., a phase-locked loop in Fig. 3, page 17, 2nd and 3rd paragraph) for generating an internal clock signal CLL2 ("Clock Signal Input" 1st row of Fig. 12) based on the external clock signal CL2i thereby compensating for a duty ratio deviation of the external clock signal CL2i (page 3, last paragraph; page 4, lines 20-23; page 6, line 9; page 15, 4th paragraph; page 50, 4th paragraph), said internal clock signal CLL2 swinging from a first voltage to a second voltage lower than the first voltage; a data storage circuit CST (Fig. 12; p. 24, line 18 to p. 25, line 5) for storing therein the internal image signal D1, D3, D5 at a timing of a voltage change from the first voltage to the second voltage as a first image signal (D1, D3, D5, 3rd row of Fig. 12) and at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal CLL2 as a second image signal (D2, D4, D6, 4th row of Fig. 12); a first data bus A (p. 25, lines 9-15) for transmitting the first image signal D1, D3, D5 from the data storage circuit; a second data bus B for transmitting the second image signal D2, D4, D6 from the data storage circuit; a voltage select circuit for selecting a voltage according with the first and the second image signals to drive the liquid display panel; and a clock signal output circuit 134 ("BB" side of Fig. 10; p. 23, 4th & 5th paragraphs) for outputting the internal clock signal (i.e., the compensated external clock data) as a subsequent external clock signal CL2o ("*A display data latch clock signal as will be output to the outside [a subsequent cascade-connected drain driver] from the drain driver 130 is indicated by CL2o.*" page 15, 3rd paragraph; Fig. 2) and for outputting the first image signal and the second image signal in sequence as a subsequent external image signal (i.e., "Data Signal Output": D1-D7, last row of Fig. 12; "*Whereby the display data bits to be externally output will be output to the outside in the order of sequence that they were input externally*" p. 26, lines 1-3) to a subsequent liquid crystal drive circuit. In particular, the clock signal output circuit 134 having a delay circuit 51 (Fig. 10; p. 24, line 3; p. 35, line 12- p. 36, line 6) which delays the internal clock signal CLL2 to become the subsequent external clock signal CL2o to the subsequent liquid crystal drive circuit so as to provide phase margins thereof in a dual-edge accept scheme.

As the clock signal duty ratio variation increases via the increase of drive circuit stages, it will finally become impossible to accept any display data at the later driver circuits. The

present invention avoid the problem by compensating the duty ratio of each external clock signal form one drive circuit to a subsequent drive circuit via a delay circuit 51 for delaying the internal clock. As shown in Fig. 12, two internal signal buses A, B are used to carry the divided image signals which better shows the difference between "the internal image signal vs. the internal clock" and "the external image signal vs. the external clock". The timing of the internal image signal synchronizes with the timing of the internal clock. In the dual edge accept/import scheme, "h*owever, as readily understandable from the timing chart shown in FIG. 12, this embodiment is such that changeover points of display data as sent from the multiplex circuit 41 are identical to the riseup point and dropdown point of the clock signal (CLL2)* (p. 35, last paragraph)*". This makes it impossible for a drain driver 130 at the next stage to take any display data into the flip-flop circuits 1-3* (p. 36, 1stparagraph)." The invention thus use the output circuit to arrange the divided internal image signals in order/sequence to be the subsequent external image signal for the next drive circuit, and uses the delay circuit to delay the internal clock into the subsequent external clock with the necessary marginal spaces or "clearances" so as to match with the subsequent external image signal. These operations were necessitated by the dual edge accept/import scheme.

The invention (Embodiment 3 in Figs. 24-25), as now recited in claim 5, is also directed to a liquid crystal display device having a liquid crystal display element 52, a plurality of cascade-connected liquid crystal drive circuits, and a plurality of signal lines formed over an edge portion of the liquid crystal display element for transmitting a signal between any two of the drive circuits. Each of the liquid crystal drive circuits comprises: a data input terminal connected with one of the signal lines to receive an external image signal being input thereto as an internal image signal into said each of the liquid crystal drive circuits; a clock compensation circuit for inputting an external clock signal and outputting an internal clock signal, the internal clock signal having a first period for outputting a first voltage and a second period for outputting a second voltage; a first data latch circuit for taking thereto the internal image signal at a timing of a voltage change from the first voltage to the second voltage of the internal cloak as a first image signal; a second data latch circuit for taking thereto the internal image signal at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal of the internal cloak as a second image signal; a first data bus for transmitting the first image signal from the first data latch circuit; a second data bus for transmitting the second image signal from the second data latch circuit; a voltage output circuit for outputting a voltage selected according with the first and

the second image signals on the first and second data buses to the liquid crystal display element; a data output circuit for outputting the image signal on the data bus to a subsequent liquid crystal drive circuit; a clock formation circuit being operable to correct a duty ratio deviation of the external clock signal to provide the internal clock signal; and a clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal and for outputting the first image signal and the second image signal in sequence as a subsequent external image signal to a subsequent liquid crystal drive circuit, said clock signal output circuit having a delay circuit. In particular, the internal clock signal is delayed to become the subsequent external clock signal by the delay circuit so as to provide phase margins thereof in a dual-edge accept scheme.

Applicants respectfully contend that neither Someya nor any other cited prior art reference teaches or suggests such "a delay circuit for delaying the internal clock signal to become the subsequent external clock signal CL2o to the subsequent liquid crystal drive circuit so as to provide phase margins thereof in a dual-edge accept scheme" as the invention.

As admitted by the Examiner (p. 4, lines 4-6 of the outstanding Office Action), Someya, Murata, and Sasaki do not disclose "a delay circuit for delaying the internal clock signal to so as to provide phase margins thereof in a dual-edge accept scheme."

The delay circuit described col. 16, lines 62-65 of Shibata is relied upon by the Examiner to teach the delay circuit of the invention. Although Shibata's delay circuit generates "*internal clock signals having the same frequency as said external clock signals but having delay relative to the external clock signals,*" it is provided in the synchronous DRAM to cancel "*the delay of signals through the input buffer* (col. 14, lines 56-57)" so as to ensure internal clock signals ***in synchronism with*** the clock signals fed from an external unit (Abstract; col. 1, lines 26-27; col. 14, lines 30-31), rather than "delaying the internal clock signal to become the subsequent external clock signal so as to **provide phase margins thereof**" as the invention. It is well established that a rejection based on cited references having principles that teach away from the invention is improper.

In particular, "*having delay relative to the external clock signals*" means Shibata either advances or delays (rather than just "delay") the phase of the internal clock signal clk to ensure it synchronizes with the external clock signal CLK. "*As the control voltage VC is raised, the delay time in the voltage-dependent delay means is shortened, whereby the phase of the internal clock signal clk is advanced (the frequency is increased) and synchronized with the external*

clock signal CLK (col. 8,lines 5-9)." "*As the control voltage VC is lowered, the delay times of the voltage-dependent delay means are lengthened and the phase of the internal clock signal clk is delayed (the frequency is decreased) so as to be synchronized with the external clock signal CLK* (col. 8, lines 15-19)." "T*he number of stages of the inverter circuits (delay circuits) constituting the ring oscillator according to this embodiment is changed in order to substantially broaden the range of operation frequencies* (col. 10, lines 58-61; col. 14, lines 48-51)."

Although the invention applies the general delay circuit, the invention applies the mechanism in "delaying the internal clock signal to become the subsequent external clock signal CL2o to the subsequent liquid crystal drive circuit so as to provide phase margins thereof in a dual-edge accept scheme" to achieve unexpected results or properties. For example, using the output circuit to arrange the divided internal image signals in order/sequence to be the subsequent external image signal for the next drive circuit, and using the delay circuit to delay the internal clock into the subsequent external clock with the necessary marginal spaces or "clearances" so as to match with the subsequent external image signal thereof in a dual-edge accept scheme. The presence of these unexpected properties is evidence of nonobviousness. MPEP§716.02(a).

> "*Presence of a property not possessed by the prior art is evidence of nonobviousness. In re Papesch, 315 F.2d 381, 137 USPQ 43 (CCPA 1963) (rejection of claims to compound structurally similar to the prior art compound was reversed because claimed compound unexpectedly possessed anti-inflammatory properties not possessed by the prior art compound); Ex parte Thumm, 132 USPQ 66 (Bd. App. 1961) (Appellant showed that the claimed range of ethylene diamine was effective for the purpose of producing " 'regenerated cellulose consisting substantially entirely of skin' " whereas the prior art warned "this compound has 'practically no effect.' ").*

Although "[t]*he submission of evidence that a new product possesses unexpected properties does not necessarily require a conclusion that the claimed invention is nonobvious. In re Payne, 606 F.2d 303, 203 USPQ 245 (CCPA 1979). See the discussion of latent properties and additional advantages in MPEP § 2145*," the unexpected properties were unknown and non-inherent functions in view of Shibata, since Shibata does not inherently achieve the same results. In other words, these advantages would not flow naturally from following the teachings of Shibata, since Shibata fails to suggest applying "a delay circuit for delaying the internal clock

signal to become the subsequent external clock signal CL2o to the subsequent liquid crystal drive circuit so as to provide phase margins thereof in a dual-edge accept scheme".

Applicants further contend that the mere fact that one of skill in the art could accidentally arrange the delay circuit of Shibata in a dual-edge accept scheme to meet the terms of the claims is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for one skilled in the art to provide the unexpected properties, such as using the output circuit to arrange the divided internal image signals in order/sequence to be the subsequent external image signal for the next drive circuit, and using the delay circuit to delay the internal clock into the subsequent external clock with the necessary marginal spaces or "clearances" so as to match with the subsequent external image signal thereof in a dual-edge accept scheme, without the benefit of appellant's specification, to make the necessary changes in the reference device. *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984). MPEP§2144.04 VI C.

Applicants contend that neither Someya nor Murata or Sasaki or Shibata teaches or discloses each and every feature of the present invention as disclosed in at least independent claims 1 and 5. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of

the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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